Claims:

1. An integrated circuit comprising:

a two-dimensional pyramid filter architecture of an order 2N-1, where N is a positive integer greater than three;

said two dimensional pyramid filter architecture of order 2N-1, in operation, capable of producing, on respective clock cycles, at least the following:

pyramid filtered output signals corresponding to output signals produced by four one-dimensional pyramid filters of order 2N-1; and

pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid filter of order [2(N-1) – 1] using signal sample matrices of order [2(N-1)-1];

wherein the respective output signals in said two dimensional pyramid filter architecture are summed on respective clock cycles of said two dimensional pyramid filter architecture.

2. The integrated circuit of claim 1, wherein N is four; and

wherein said two dimensional pyramid filter architecture of order seven, in operation, capable of producing, on respective clock cycles, the pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid of order five using four signal sample matrices $P^{5x5}_{i-1,j-1}, P^{5x5}_{i-1,j+1}, P^{5x5}_{i+1,j-1}, P^{5x5}_{i+1,j+1}$, the pyramid filtered output signals being produced by a plurality of one-dimensional pyramid filters.

3. The integrated circuit of claim 2, wherein said one-dimensional pyramid filters comprise a sequence of scalable cascaded multiplerless operational units, each of said operational units capable of producing a different order pyramid filtered output signal sample stream.

4. The integrated circuit of claim 2, wherein said one-dimensional pyramid filters comprise other than one-dimensional multiplierless pyramid filters.

5. The integrated circuit of claim 2, wherein said two dimensional

pyramid filter architecture of order seven, in operation, capable of producing, on respective clock cycles, the pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid of order five using four signal sample matrices $P^{5x5}_{i-1,j-1}, P^{5x5}_{i-1,j+1}, P^{5x5}_{i+1,j-1}, P^{5x5}_{i+1,j+1}$, the pyramid filtered output signals produced by a plurality of one-dimensional pyramid filters being produced by eight one-dimensional pyramid filters of order five.

6. The integrated circuit of claim 5, wherein, of the eight one-dimensional pyramid filters of order five, four are applied row-wise and four are applied column-wise.

7. The integrated circuit of claim 5, wherein said two dimensional pyramid filter architecture of order seven, in operation, capable of producing, on respective clock cycles, the pyramid filtered output signals corresponding to output signals produced by four two-dimensional pyramid filters of order five, the pyramid filtered output signals produced by a plurality of one-dimensional pyramid filters being produced by eight one-dimensional multiplierless pyramid filters of order five.

8. The integrated circuit of claim 7, wherein, of the eight one-dimensional pyramid filters of order five, four are applied row-wise and four are applied column-wise.

9. The integrated circuit of claim 2, wherein said two dimensional pyramid filter architecture of order seven, in operation, capable of producing, on respective clock cycles, the pyramid filtered output signals corresponding to output signals produced by four two-dimensional pyramid filters of order five, the pyramid filtered output signals produced by a plurality of one-dimensional pyramid filters being produced by other than one-dimensional multiplierless pyramid filters.

10. The integrated circuit of claim 1, wherein N is four;

said two dimensional pyramid filter architecture of order seven, in operation, being capable of producing, on respective clock cycles, at least the following:

output signals produced by four two-dimensional pyramid filters of order five.

11. The integrated circuit of claim 1, wherein said two dimensional pyramid filter architecture of order seven, in operation, capable of producing, on respective clock cycles, the pyramid filtered output signals corresponding to output signals produced by four two-dimensional pyramid filters of order five, the pyramid filtered output signals being produced by one or more two-dimensional pyramid filters other than four two-dimensional pyramid filters.

12. A method of filtering an image using a two-dimensional pyramid filter architecture of order 2N-1, where N is a positive integer greater than three, said method comprising:

summing, on respective clock cycles of said two dimensional pyramid filter architecture, the following:

pyramid filtered output signals corresponding to output signals produced by four one-dimensional pyramid filters of order 2N-1; and

pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid filter of order [2(N-1) – 1] using signal sample

matrices of order [2(N-1)-1].

13. The method of claim 12, wherein N is four;

pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid filter of order [2(N-1) – 1] using signal sample matrices of order [2(N-1)-1] comprising output signals produced by four two-dimensional pyramid filters of order five.

14. The method of claim 12, wherein N is four; and

wherein the pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid filter of order five using four signal sample matrices $P^{5x5}_{i-1,j-1}, P^{5x5}_{i-1,j+1}, P^{5x5}_{i+1,j-1}, P^{5x5}_{i+1,j+1}$ comprise pyramid filtered output signals produced by a plurality of one-dimensional pyramid filters.

15. The method of claim 14, wherein said one-dimensional pyramid filters comprise a sequence of scalable cascaded multiplerless operational

units, each of said operational units capable of producing a different order pyramid filtered output signal sample stream.

16. An article comprising: a storage medium, said storage medium having stored thereon instructions, that, when executed result in filtering an image using a two-dimensional pyramid filter architecture of order 2N-1, where N is a positive integer greater than three, by:

summing, on respective clock cycles of said two dimensional pyramid filter architecture, the following:

pyramid filtered output signals corresponding to output signals produced by four one-dimensional pyramid filters of order 2N-1; and

pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid filter of order [2(N-1) – 1] using signal sample matrices of order [2(N-1)-1].

17. The article of claim 16, wherein N is four;

pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-

dimensional pyramid filter of order [2(N-1) – 1] using signal sample matrices of order [2(N-1)-1] comprising output signals produced by four two-dimensional pyramid filters of order five.

18. The article of claim 16, wherein N is four; and

wherein the pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid of order five using four signal sample matrices $P^{5x5}_{i-1,j-1}, P^{5x5}_{i-1,j+1}, P^{5x5}_{i+1,j-1}, P^{5x5}_{i+1,j+1}$, comprise pyramid filtered output signals produced by a plurality of one-dimensional pyramid filters.

19. The article of claim 18, wherein said one-dimensional pyramid filters comprise a sequence of scalable cascaded multiplerless operational units, each of said operational units capable of producing a different order pyramid filtered output signal sample stream.

20. An image processing system comprising:

an image processing unit to filter scanned color images;

said image processing unit including at least one two-dimensional

pyramid filter architecture;

said at least one two-dimensional pyramid filter architecture comprising:

a two-dimensional pyramid filter architecture of an order 2N-1, where N is a positive integer greater than three;

said two dimensional pyramid filter architecture of order 2N-1, in operation, capable of producing, on respective clock cycles, at least the following:

pyramid filtered output signals corresponding to output signals produced by four one-dimensional pyramid filters of order 2N-1; and

pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid filter of order [2(N-1) – 1] using signal sample matrices of order [2(N-1)-1];

wherein the respective output signals in said two dimensional pyramid filter architecture are summed on respective clock cycles of said two dimensional pyramid filter architecture.

21. The system of claim 20, wherein N is four;

pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid filter of order [2(N-1) – 1] using signal sample matrices of order [2(N-1)-1] comprising output signals produced by four two-dimensional pyramid filters of order five.

22. The system of claim 20, wherein N is four; and

wherein the pyramid filtered output signals corresponding to output signals produced either by four two-dimensional pyramid filters or one two-dimensional pyramid of order five using four signal sample matrices $P^{5x5}_{i-1,j-1}, P^{5x5}_{i-1,j+1}, P^{5x5}_{i+1,j-1}, P^{5x5}_{i+1,j+1}$, comprise pyramid filtered output signals produced by a plurality of one-dimensional pyramid filters.

23. The system of claim 22, wherein said one-dimensional pyramid filters comprise a sequence of scalable cascaded multiplerless operational units, each of said operational units capable of producing a different order pyramid filtered output signal sample stream.